Professor Oliver Chyan

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Biographical Sketch

Professor Chyan's research program has an international reputation of successfully exploring critical underlying fundamental interfacial science to greatly facilitate microelectronic fabrication and functional nanostructure design development. Professor Chyan received his Ph.D. degree in materials chemistry from MIT. Since 1992, Chyan established *the Interfacial Electrochemistry and Materials Research laboratory* where he leads an interdisciplinary research team to investigate multitude of fundamental and applied research projects relevant to semiconductor processing and advanced microelectronic fabrication. **For front end processing**, detection and monitoring of metal and organic contamination in various wet clean solutions were carried out to achieve ultraclean silicon surface. Exploring novel wet clean chemistry on 2D TMD materials to facilitate high-yield nanoelectronics fabrication. **Relating to the back end processing**, Dr. Chyan invented an ultra-thin, directly-plate-able Ru-based Cu diffusion barrier/liner for advanced interconnect application. Important interfacial phenomena including Cu ECD back fill, Cu diffusion, Cu post CMP clean and Cu/Ru bimetallic corrosion were actively investigated. Novel spectroscopic metrology was developed to characterize trace post-etch residues on patterned ultra-low k nanostructure. New insights obtained on the chemical, structural and bonding modification across ULK ILD interfaces has facilitated development of plasma etching and post etch cleaning techniques that minimize low-k dielectric damage. Current BEOL/MEOL research efforts is centered on optimizing interfacial chemistry control to facilitate fabrication of nano-interconnects using Ru and Mo. **In IC packaging area**, Dr. Chyan's team developed a novel Cu-selective passivation coating that eliminates chloride induced corrosion defects of Cu wire bonding packaging under thermal stress. Active exploration is in progress to apply this Cu-selective coating technology to advanced 2D/3D IC packaging. New fabrication technology of high-density Cu Interconnect for advanced IC packaging is also actively explored. Dr. Chyan's research program was supported by Semiconductor Research Corporation and industrial partners including Intel, TI, TEL, NXP/Freescale, Lam Research, MediaTek, L-3 Communications, ATMI, JSR-micro, and REC Inc.

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Highlights of Industrial Collaboration Research Activities:

- Over 30 years of research expertise in material chemistry and interfacial characterization related to microelectronics fabrication and process integration.

- Specialized in Interfacial Engineering across whole spectrum of IC fabrication processes: Front End of Line, Middle End of line, Back End of Line and IC Packaging
- Strong partnership with major IC companies: Intel, TSMC, GlobalFoundries, TI, Lam Research, TEL, NXP/Freescale, MediaTek, ATMI/Entegris, JSR Micro, and L-3 Communications.
- Mentored Graduate Students graduated from PI's lab: Thirty-one. (>85% employed by microelectronic company)
- Achieved the largest technology Transfer agreement in the UNT history from Intel to acquire PI's patented highly sensitive wafer characterization technology (US Patent # 9,366,601). (**Intel**).
- Invent Silicon -based impurities senor (U.S. Patent 6,145,372) to aid FEOL chemical processing control (**TI**).
- Invent monitoring tool to precisely control on the Cu etching rate for high density interconnects fabrication (U.S. Patent 11,099,131) in advanced IC packaging application. (**Intel**)
- Invent Ru-based liner/barrier (U.S. Patent 7,247,554) that is directly plate-able with Cu. (**TI, SRC**).
- Explore a better understanding of fundamental corrosion mechanism of Cu wire bonded Al bond pad to aid the practical packaging process designs for improved reliability (**NXP, Freescale, TI , SRC**).
- Invent a highly sensitive Cu-selective passivation coating that achieved high corrosion protection for IC packaging. Completed a pilot production trial that passed all stringent reliability test requirements. (**NXP, Mindox Techno**)

Invention and Technology Transfer from Professor Chyan's Group

Four United States Patents (*US Patent*# 6145372, 7247554, 9366601 and 11099131) were awarded to professor Chyan's invention. Three additional US Provisional Patents #62/432115, #62/511863 and #62/897942 have been filed by UNT based on Chyan team's technology.

- ***US Patent*# 9366601 (Novel Chemical Bonding Transformation Mapping Probe based on MIR-IR)** has received >$2, 215, 000 external funding. The original invention results in 15 publications, 11 professional presentation and 15 invited talks. This patented wafer characterization technology received the largest technology transfer from a major microelectronic company in UNT history.

- ***US Patent*# 6145372 (Detection of Trace Contamination on Silicon wafer)** has attracted >$523,000 external funding. The original invention results in 9 publications, 14 professional presentation and 15 invited talks.

- ***US Patent*# 7247554 (New Ru-based Cu Diffusion Barrier and Cu/Ru Bimetallic Corrosion)** has attracted >$1,340,000 external funding. The original invention contributed to 14 publications, 40 professional presentation and 12 invited talks.

- ***US Patent # 11099131* (New Monitoring Metrology for Precise Cu Etching Control)** has awarded with a $190,000/2 years funding support form Intel. CHEMCUT Inc. has expressed interested in technical transfer negotiation and licensing request to UNT. Report in 1 publication and 3 presentation.

- ***US Provisional Patent Application* #62/511863 (Corrosion Prevention Treatments for Wire Bonded Semiconductor Assembly)** has attracted >$1,558,000 external funding. The Changzhou Ruize Microelectronics Co. (REC) has requested tech transfer licensing of this PI's invention. The original invention contributed to 3 publications, 3 professional presentation and 5 invited talks.

Recent Selected Publications with Collaborating Industrial Partners

1. "Exploration of Interfacial Materials Chemistry Control to Improve Cu Wire Bonding Reliability **"** Antony Jesu Durai, K.; Kumaravel, D. K.; Alptekin, J.; Estridge, L.; Nair, S.; Chyan, O.M.R., *Journal of Microelectronics and Electronic Packaging*, **2024**, *21* (2): 42-49. **(NXP)**

2. "Cu-Cu Wire-Bonding Enabled by a Cu-selective Passivation Coating to Enhance Packaging Reliability " Alptekin, J.; Antony Jesu Durai, K.; Kumaravel, D. K.; Estridge, L.; Chyan, O.M.R., Ibrahim, R.; Li, G. M., Mathew, V. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2023**, 13, 1923-1928. **(NXP)**

3. "Prevention of Cu Electrolytic Migration Defects on RDL by a Cu-selective Passivation to Enhance Reliability **"** Salunke, A.; Akula, K.; Jayakumar, S.; Kumar, S.; Alptekin, J.; Chyan, O.M.R., *Journal of Microelectronics and Electronic Packaging*, **2023**, *20*, 17–26. **(TI)**

4. "Comparative Study of Chloride and Fluoride Induced Aluminum Pad Corrosion in Wire-Bonded Device Packaging Assembly" Ashok Kumar, G. I.; Lambert, A; Caperton, J; Asokan, M.; Yi, W.; Chyan, O.M.R., *Corros. Mater. Degrad.* **2021**, 2, 447–460. **(Intel, SRC)**

5. "Mechanistic study of copper wire-bonding failures on packaging devices in acidic chloride environments" Ross, N.; Asokan, M.; Ashok Kumar, G. I.; Caperton, J.; Alptekin, J.; Salunke, A. S.; Chyan, O.M.R., *Microelectronics Reliability*, **2020**, 113, 113917. **(NXP, SRC)**

6. "Thin-Film UV-Vis Spectroscopy as a Chemically-Sensitive Monitoring Tool for Copper Etching Bath" Lambert, A.; Asokan, M.; Goutham, I.; Love, C.; Chyan, O., *Journal of Industrial and Engineering Chemistry*, **2017**, 51, 44–48. **(Intel)**

7. "Micro-pattern Corrosion Screening on Bimetallic Corrosion for Microelectronic Application" Yu, K.; Rimal, S,; Asokan, M.; Nalla, P.; Koskey, S.; Pillai, K.; Chyan, O.; Singh, K.J.; Suri, S.; *Electrochemica Acta*, **2016**, *210*, 512-519. **(Intel, SRC)**

8. *"Exploration of Chemical Bonding Transformation Mapping to Assist Low-k Dielectric Nanostructure Fabrication"* Rimal, S.; Mukherjee, T.; Goswami, A.; Ross, N.; Chyan, O.; *ECS Transactions*, **2015**, *66*, 1-13. **(Intel, TEL)**

9. *"UV-assisted Modification and Removal Mechanism of a Fluorocarbon Polymer Film on Low-k Dielectric Trench Structure"* Mukherjee, T.; Berhe, S.A.; Goswami, A.; Chyan, O.; Singh, K. J.; Brown, I., *ACS Appl. Mater. Interfaces*, **2015**, 7, 5051-5055. **(Intel, TEL)**

10. *"Evaluation of plasma damage to low-k dielectric trench structures by multiple internal reflection infrared spectroscopy"* Rimal, S.; Mukherjee, T.; Abdelghani, J.; Goswami, A.; Chyan, O.; Stillahn, J.; Chiba, Y.; Maekawa, K., *ECS Solid State Letters* **2014**, 3(3), N1-N4. **(TEL)**

11. *"Bonding Structure of Model Fluorocarbon Polymer Residue Determined by Functional Group Specific Chemical Derivatization"* Mukherjee, T.; Rimal, S. ; Koskey, S.; Chyan, O.; Singh, K.J., Myers, A.M., *ECS Solid State Letters,* **2013**, 2(3), N11-N14. **(Intel)**

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